PIC12F629/675

EEPROM Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC12F629
- PIC12F675

1.0 PROGRAMMING THE PIC12F629/675

The PIC12F629/675 is programmed using a serial method. The Serial mode will allow the PIC12F629/675 to be programmed while in the user's system. This allows for increased design flexibility. This programming specification applies to PIC12F629/675 devices in all packages.

1.1 Hardware Requirements

The PIC12F629/675 requires one power supply for VDD (5.0V) and one for VPP (12V).

1.2 Programming Mode

The Programming mode for the PIC12F629/675 allows programming of user program memory, data memory, special locations used for ID, and the configuration word.

FIGURE 1-1: 8-PIN DIAGRAM FOR PIC12F629/675

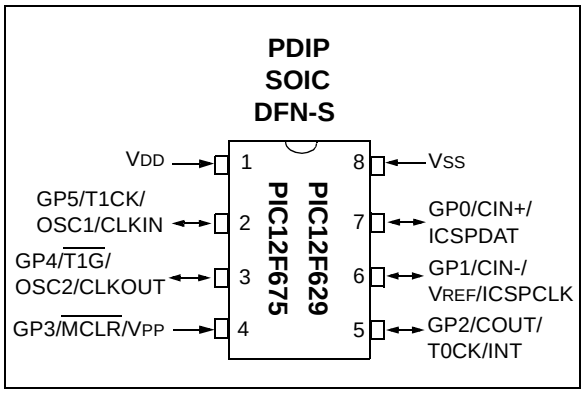


TABLE 1-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC12F629/675

Pin Name	During Programming		
	Function	Pin Type	Pin Description
GP1	CLOCK	I	Clock input – Schmitt Trigger input
GP0	DATA	I/O	Data input/output – TTL input
MCLR	Programming mode	P*	Program Mode Select
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

* In the PIC12F629/675, the programming high voltage is internally generated. To activate the Programming mode, high voltage needs to be applied to MCLR input. Since the MCLR is used for a level source, this means that MCLR does not draw any significant current.

2.0 PROGRAM MODE ENTRY

2.1 User Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF. In Programming mode, the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The PC will increment from 0x0000 to 0x1FFF and wrap to 0x000, 0x2000 to 0x3FFF and wrap around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to RESET the part and re-enter Program/Verify mode as described in Section 2.3.

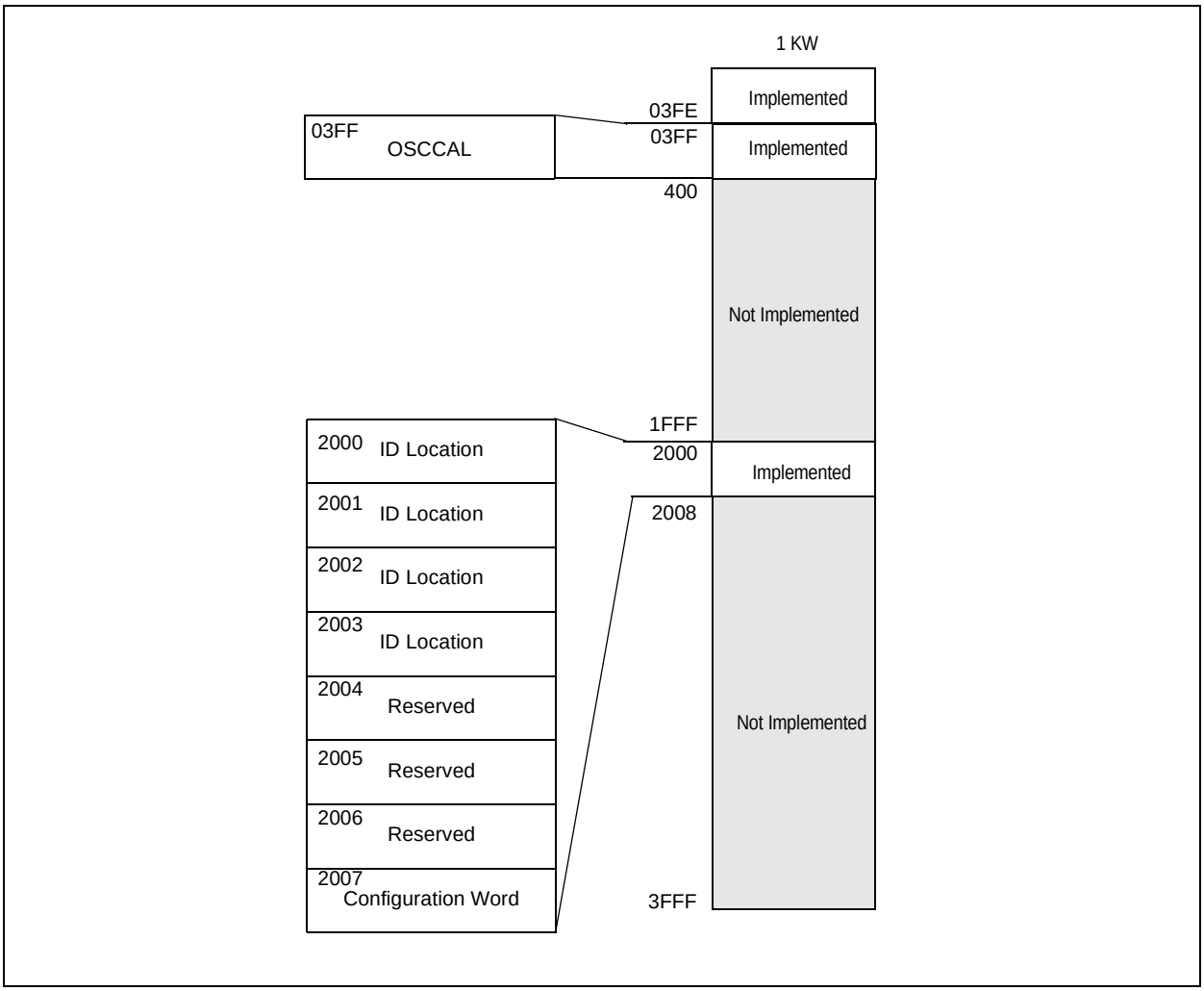
In the configuration memory space, 0x2000-0x200F are physically implemented. However, only locations 0x2000 through 0x2003, and 0x2007 are available. Other locations are reserved.

2.2 ID Locations

A user may store identification information (ID) in four ID locations. The ID locations are mapped in [0x2000 : 0x2003]. It is recommended that the user use only the seven Least Significant bits of each ID location. Locations read out normally, even after code protection. The ID locations read out in an unscrambled fashion after code protection is enabled. It is recommended that ID location is written as "xx xxxx xbbb bbbb" where 'bbb bbbb' is ID information.

The 14 bits may be programmed, but only the LSb's are displayed by MPLAB® IDE. xxxx's are "don't care" bits as they won't be read by MPLAB IDE.

FIGURE 2-1: PROGRAM MEMORY MAPPING

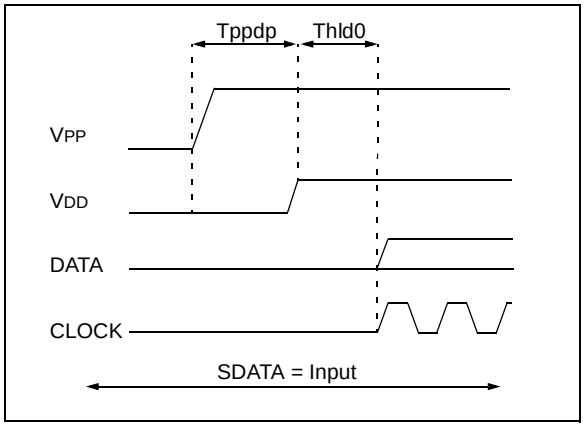


2.3 Program/Verify Mode

The Program/Verify mode is entered by holding pins CLOCK and DATA low while raising $\overline{MCLR}$ pin from V_{IL} to V_{IHH} (high voltage). Apply V_{DD} and data. Once in this mode, the user program memory, data memory and the configuration memory can be accessed and programmed in serial fashion. CLOCK is Schmitt Trigger and DATA is TTL input in this mode. GP4 is tristate, regardless of fuse setting.

The sequence that enters the device into the Programming/Verify mode places all other logic into the RESET state (the $\overline{MCLR}$ pin was initially at V_{IL}). This means that all I/O are in the RESET state (hi-impedance inputs).

FIGURE 2-2: ENTERING HIGH VOLTAGE PROGRAM/VERIFY MODE



The normal sequence for programming is to use the LOAD DATA command to set a value to be written at the selected address. Issue the BEGIN PROGRAMING command followed by READ DATA command to verify and then increment the address.

A device RESET will clear the PC and set the address to '0'. The INCREMENT ADDRESS command will increment the PC. The LOAD CONFIGURATION command will set the PC to 0x2000. The available commands are shown in Table 2-1.

2.3.1 SERIAL PROGRAM/VERIFY OPERATION

The CLOCK pin is used as a clock input pin, and the DATA pin is used for entering command bits and data input/output during serial operation. To input a command, the clock pin (CLOCK) is cycled six times. Each command bit is latched on the falling edge of the clock with the Least Significant bit (LSb) of the command being input first. The data on pin DATA is required to have a minimum setup and hold time (see AC/DC specifications), with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay of 1 μs between the command and the data. After this delay, the clock pin is cycled 16 times with the first cycle being a START bit and the last cycle being a STOP bit. Data is also input and output LSb first.

Therefore, during a read operation the LSb will be transmitted onto pin DATA on the rising edge of the second cycle, and during a load operation the LSb will be latched on the falling edge of the second cycle. A minimum 1 μs delay is also specified between consecutive commands.

All commands are transmitted LSb first. Data words are also transmitted LSb first. The data is transmitted on the rising edge and latched on the falling edge of the clock. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1 μs is required between a command and a data word (or another command).

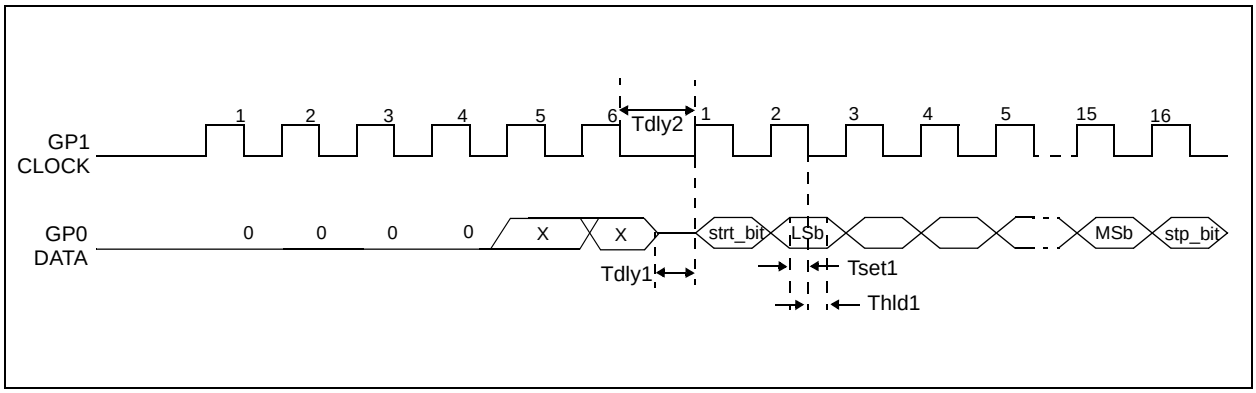
TABLE 2-1: COMMAND MAPPING FOR PIC12F629/675

Command	Mapping (MSb … LSb)						Data
LOAD CONFIGURATION	X	X	0	0	0	0	0, data (14), 0
LOAD DATA FOR PROGRAM MEMORY	X	X	0	0	1	0	0, data (14), 0
LOAD DATA FOR DATA MEMORY	X	X	0	0	1	1	0, data (8), zero (6), 0
READ DATA FROM PROGRAM MEMORY	X	X	0	1	0	0	0, data (14), 0
READ DATA FROM DATA MEMORY	X	X	0	1	0	1	0, data (8), zero (6), 0
INCREMENT ADDRESS	X	X	0	1	1	0	
BEGIN PROGRAMMING	0	0	1	0	0	0	
BULK ERASE PROGRAM MEMORY	X	X	1	0	0	1	
BULK ERASE DATA MEMORY	X	X	1	0	1	1	

2.3.1.1 LOAD CONFIGURATION

After receiving this command, the program counter (PC) will be set to 0x2000. Then, by applying 16 cycles to the clock pin, the chip will load 14 bits in a “data word,” as described above, which will be programmed into the configuration memory. A description of the memory mapping schemes of the program memory for normal operation and Configuration mode operation is shown in Figure 2-1. After the configuration memory is entered, the only way to get back to the user program memory is to exit the Program/Verify mode by taking $\overline{MCLR}$ low (V_{IL}).

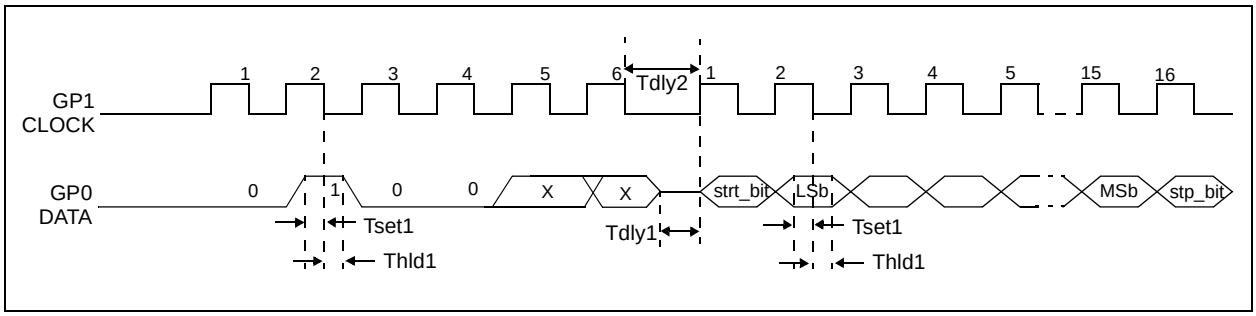
FIGURE 2-3: LOAD CONFIGURATION COMMAND



2.3.1.2 LOAD DATA FOR PROGRAM MEMORY

After receiving this command, the chip will load in a 14-bit “data word” when 16 cycles are applied, as described previously. A timing diagram for the LOAD DATA command is shown in Figure 2-4.

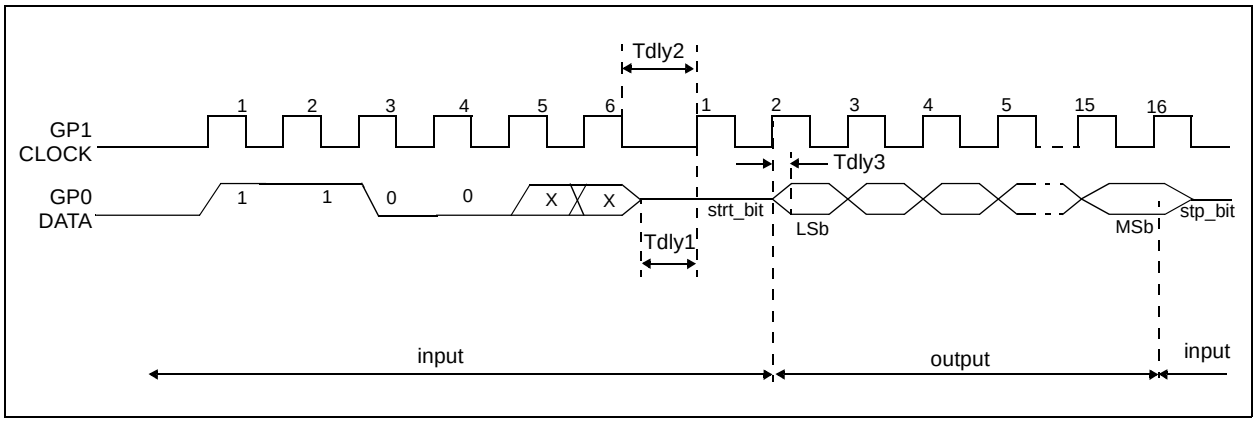
FIGURE 2-4: LOAD DATA FOR PROGRAM MEMORY COMMAND



2.3.1.3 LOAD DATA FOR DATA MEMORY

After receiving this command, the chip will load in a 14-bit “data word” when 16 cycles are applied. However, the data memory is only 8 bits wide and thus, only the first 8 bits of data after the START bit will be programmed into the data memory. It is still necessary to cycle the clock the full 16 cycles in order to allow the internal circuitry to reset properly. The data memory contains 128 bytes. Only the lower 8 bits of the PC are decoded by the data memory, and therefore, if the PC is greater than 0x7F, it will wrap around and address a location within the physically implemented memory.

FIGURE 2-5: LOAD DATA FOR DATA MEMORY COMMAND

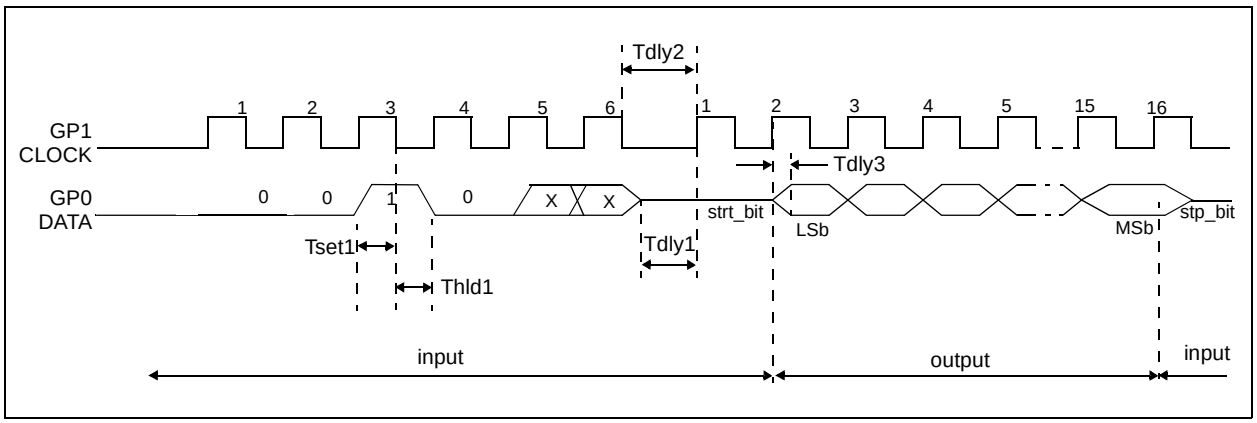


2.3.1.4 READ DATA FROM PROGRAM MEMORY

After receiving this command, the chip will transmit data bits out of the program memory (user or configuration) currently accessed, starting with the second rising edge of the clock input. The DATA pin will go into Output mode on the second rising clock edge, and it will revert to Input mode (hi-impedance) after the 16th rising edge.

If the program memory is code protected ($\overline{CP}$ = 0), the data is read as zeros.

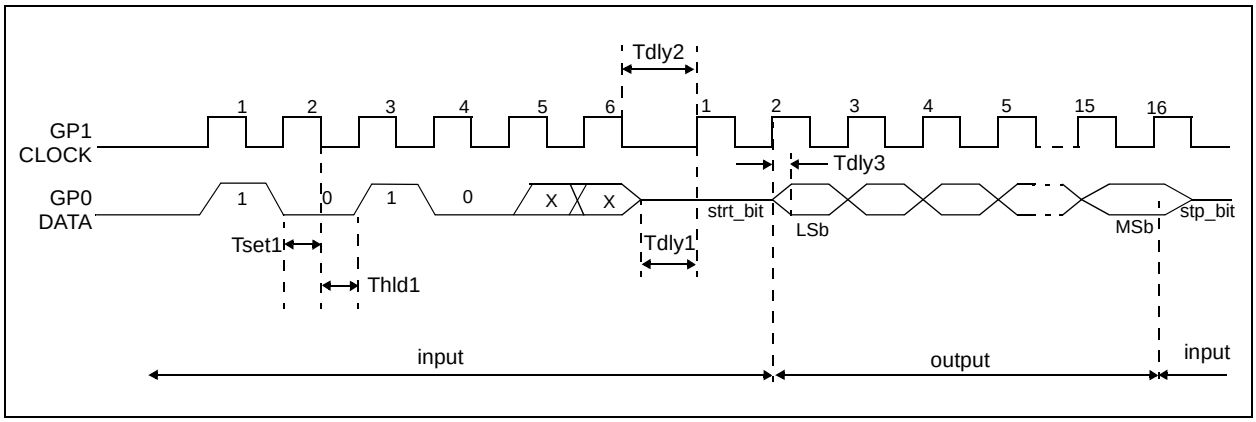
FIGURE 2-6: READ DATA FROM PROGRAM MEMORY COMMAND



2.3.1.5 READ DATA FROM DATA MEMORY

After receiving this command, the chip will transmit data bits out of the data memory starting with the second rising edge of the clock input. The DATA pin will go into Output mode on the second rising edge, and it will revert to Input mode (hi-impedance) after the 16th rising edge. As previously stated, the data memory is 8 bits wide, and therefore, only the first 8 bits that are output are actual data. If the data memory is code protected, the data is read as all zeros. A timing diagram of this command is shown in Figure 2-7.

FIGURE 2-7: READ DATA FROM DATA MEMORY COMMAND

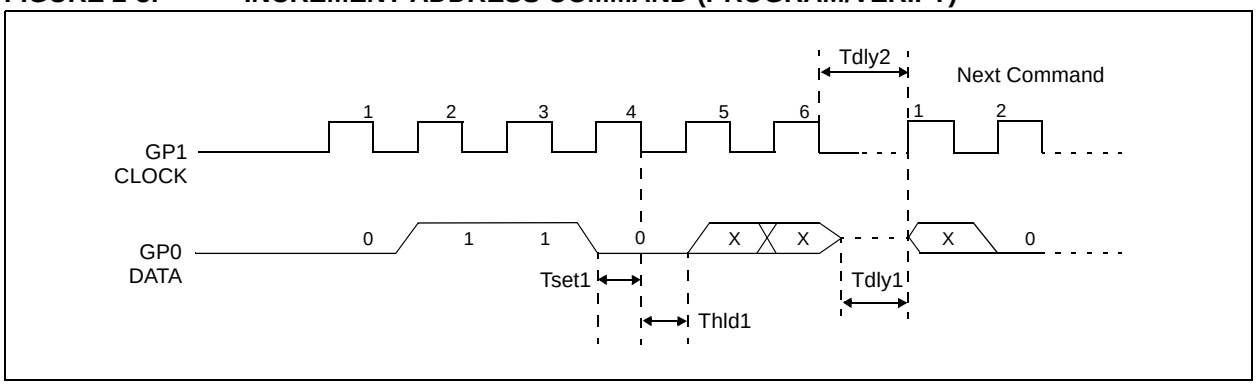


2.3.1.6 INCREMENT ADDRESS

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 2-8.

It is not possible to decrement the address counter. To reset this counter, the user should exit and re-enter Programming mode.

FIGURE 2-8: INCREMENT ADDRESS COMMAND (PROGRAM/VERIFY)

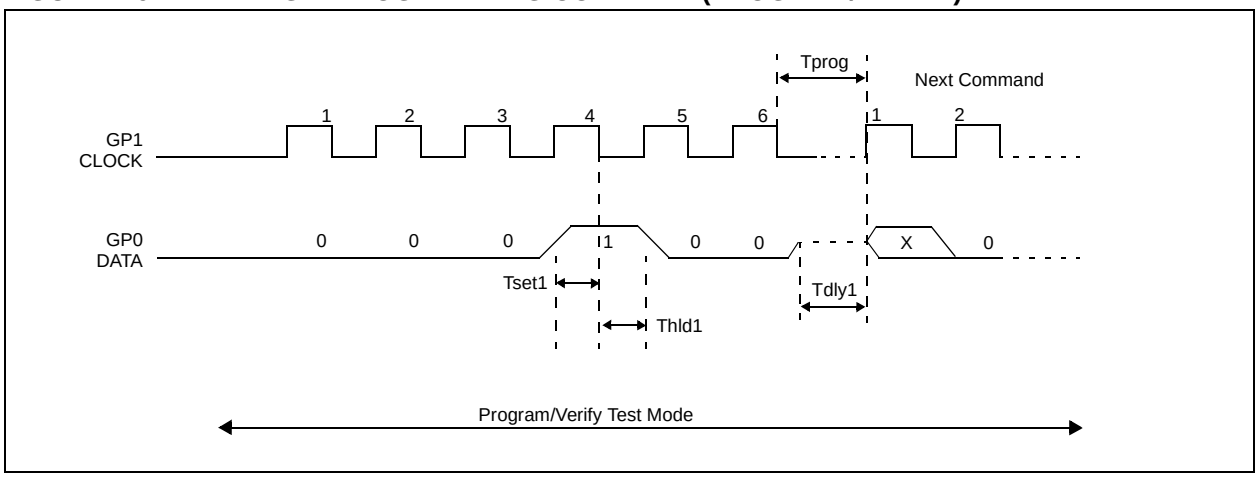


2.3.1.7 BEGIN PROGRAMMING

A load command must be given before every BEGIN PROGRAMMING command. Programming of the appropriate memory (user program memory or data memory) will begin after this command is received and decoded. An internal timing mechanism executes a write. The user must allow for program cycle time for programming to complete. No END PROGRAMMING command is required.

When programming data memory, the byte being addressed is erased before being programmed.

FIGURE 2-9: BEGIN PROGRAMMING COMMAND (PROGRAM/VERIFY)



2.3.1.8 BULK ERASE PROGRAM MEMORY

After this command is performed and calibration bits are erased, the entire program memory is erased. If data is code protected, data memory will also be erased.

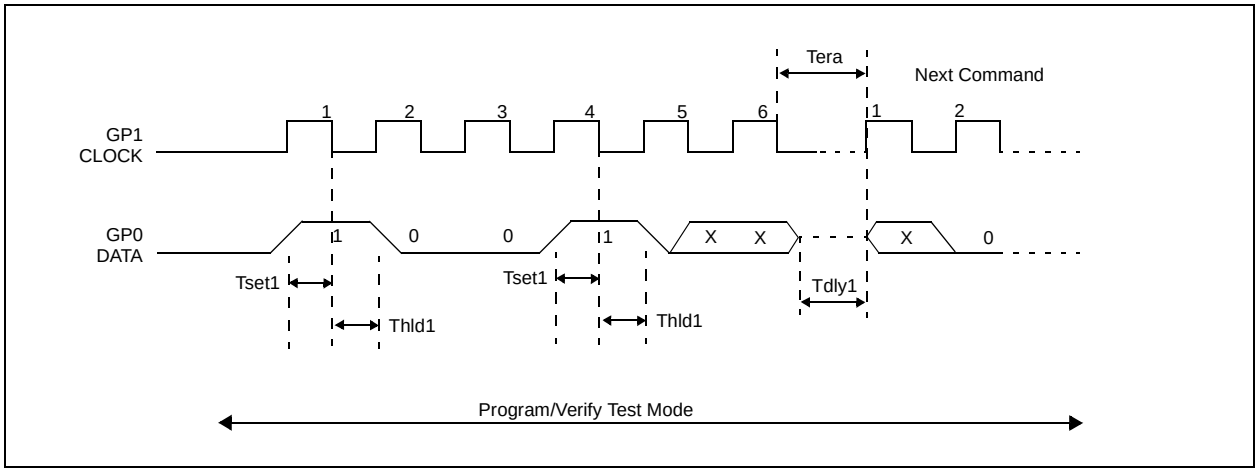
Note:	The OSCCAL word and BG bits must be read prior to erasing the device and restored during the programming operation. OSCCAL is at location 0x3FF and the BG bits are bits 12 and 13 of the configuration word (0x2007).

To perform a bulk erase of the program memory, the following sequence must be performed.

1. Read OSCCAL 0x3FF.
2. Read configuration word.
3. Do a BULK ERASE PROGRAM MEMORY command.
4. Wait Tera to complete bulk erase.

If the address is pointing to the ID/configuration program memory (0x2000 - 0x200F), then both the user memory and the ID locations will be erased.

FIGURE 2-10: BULK ERASE PROGRAM MEMORY COMMAND



2.3.1.9 BULK ERASE DATA MEMORY

To perform a bulk erase of the data memory, the following sequence must be performed.

1. Do a BULK ERASE DATA MEMORY command.
2. Wait Tera to complete bulk erase.

Data memory won't erase if code protected ($\overline{CPD}$ = 0).

Note: All BULK ERASE operations must take place at 4.5V to 5.5V V_{DD} range for PIC12F629/675 devices and 2.0V to 5.5V V_{DD} for PIC12F629/675-ICD devices.

FIGURE 2-11: BULK ERASE DATA MEMORY COMMAND

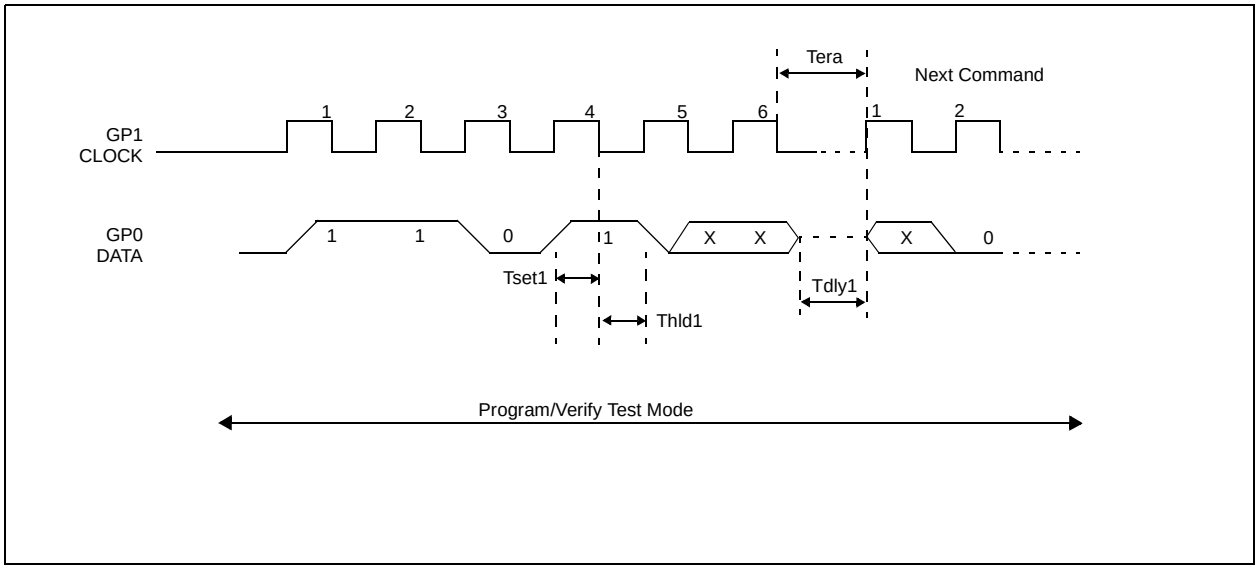


FIGURE 2-12: PROGRAM FLOW CHART - PIC12F629/675 PROGRAM MEMORY

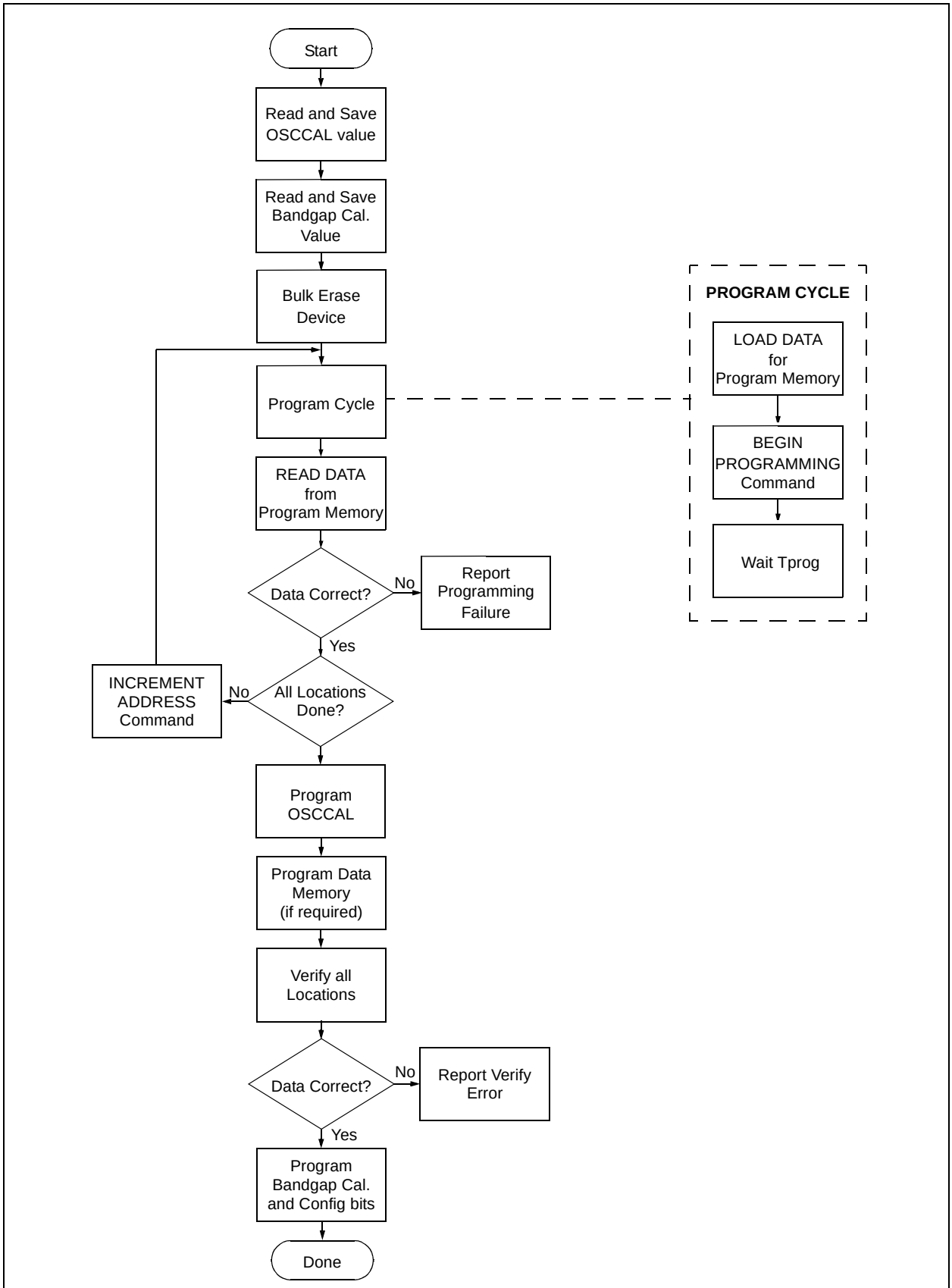


FIGURE 2-13: PROGRAM FLOW CHART - PIC12F629/675 CONFIGURATION MEMORY

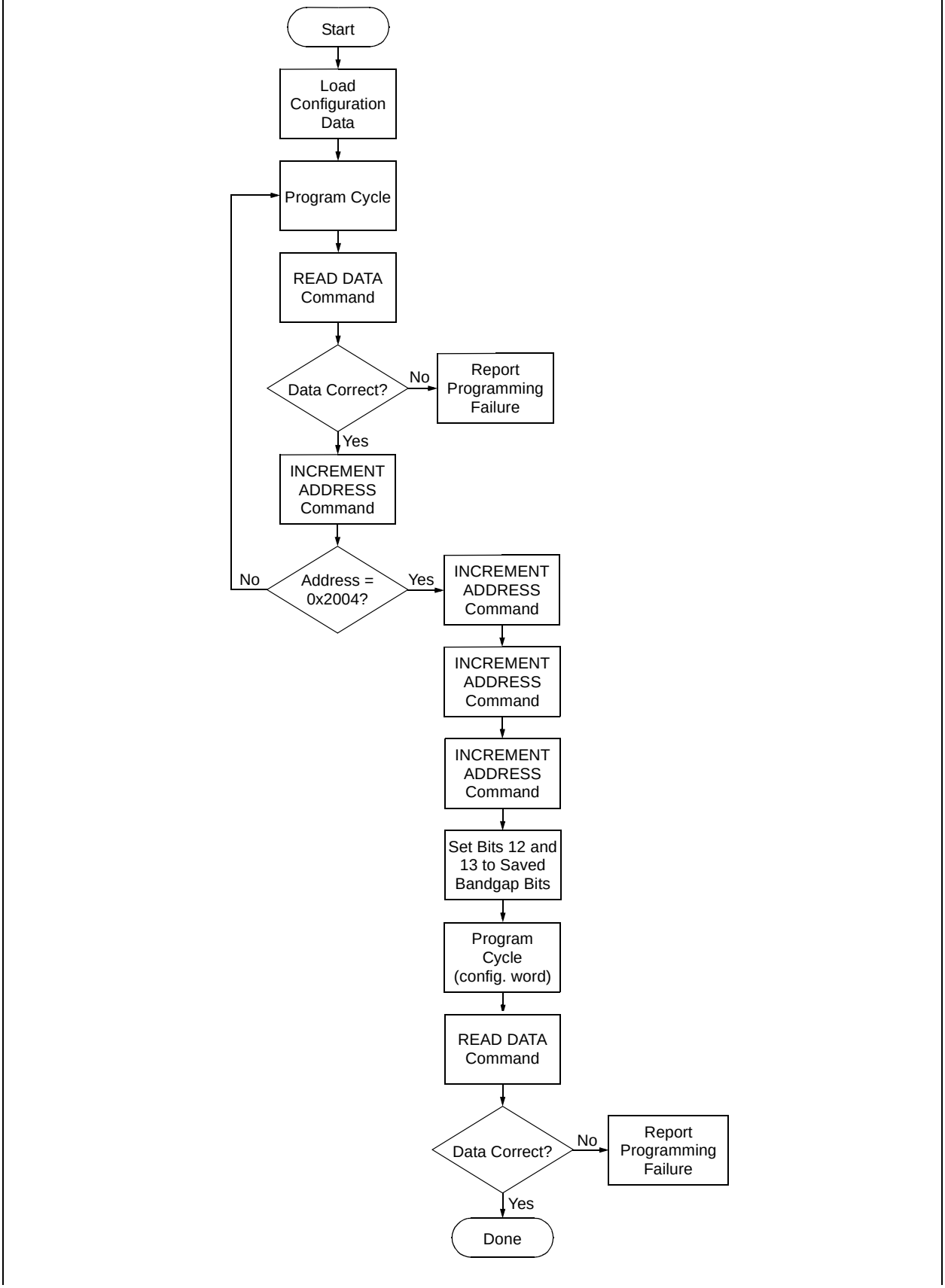


FIGURE 2-14: PROGRAM FLOW CHART - PIC12F629/675 DATA MEMORY

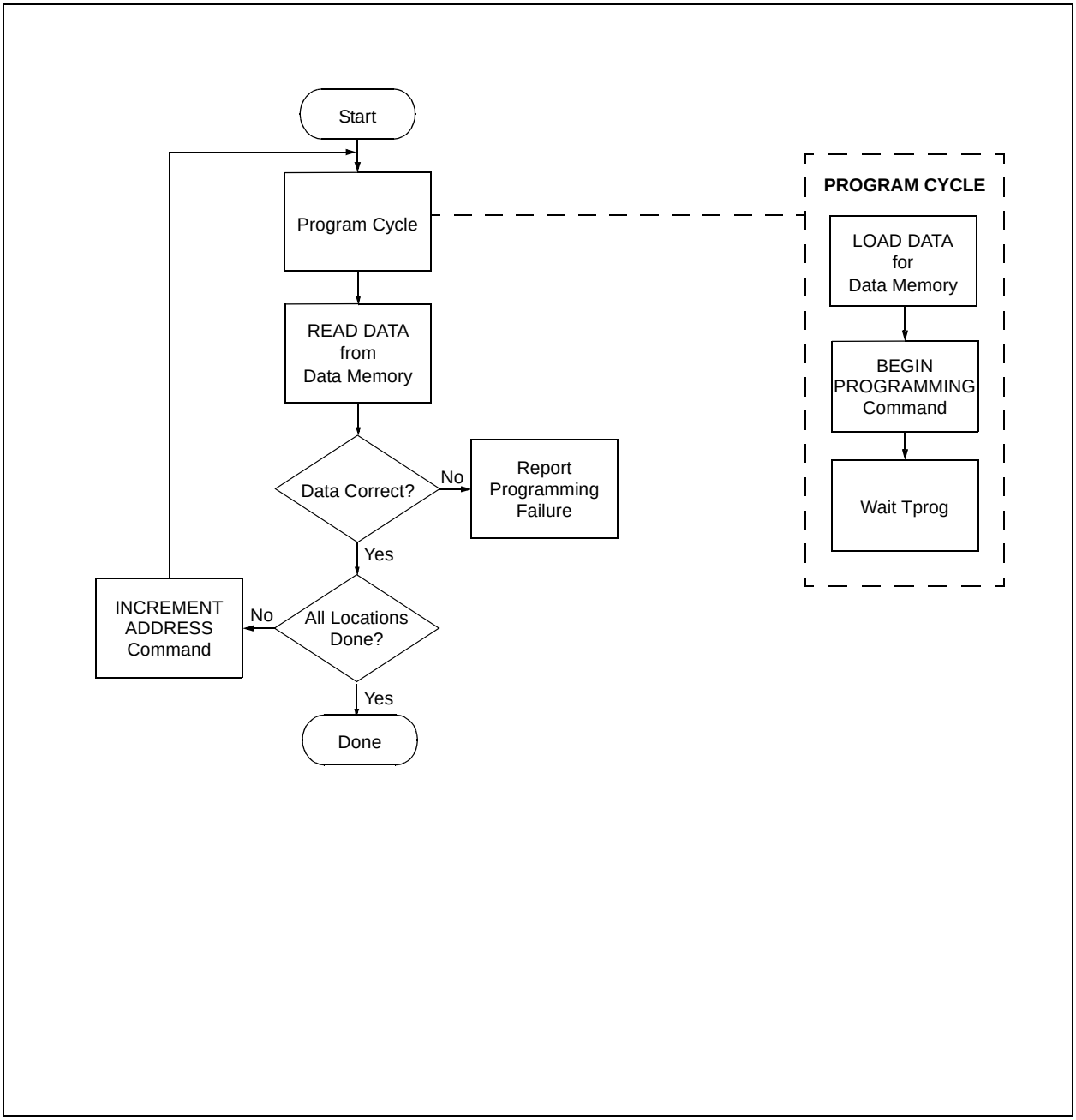
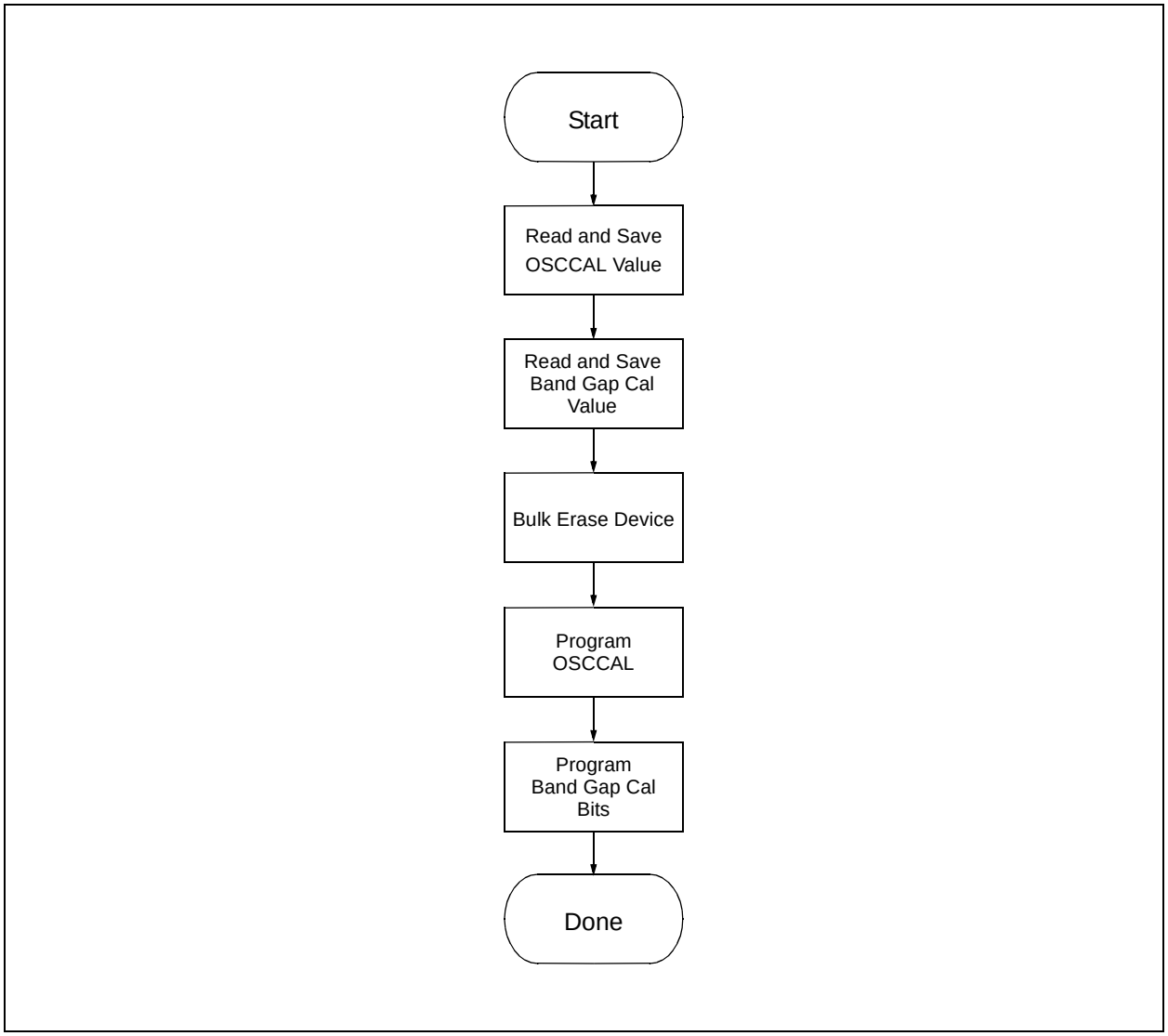


FIGURE 2-15: PROGRAM FLOW CHART - ERASE FLASH DEVICE



3.0 CONFIGURATION WORD

The PIC12F629/675 has several configuration bits. These bits can be programmed (reads '0'), or left unchanged (reads '1'), to select various device configurations.

REGISTER 3-1: CONFIGURATION WORD FOR PIC12F629/675 DEVICE

R/P-1	R/P-1	U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
BG1	BG0	—	—	—	$\overline{CPD}$	$\overline{CP}$	BODEN	MCLRE	$\overline{PWRTE}$	WDTE	FOSC2	F0SC1	F0SC0
bit 13													bit 0

bit 13-12 **BG<1:0>**: Bandgap Calibration bits(2)
00 = Lowest Bandgap voltage
...
11 = Highest Bandgap voltage

bit 11-9: **Unimplemented**: Read as '0'

bit 8: **$\overline{CPD}$**: Code Protection Data
1 = Data memory is not protected
0 = Data memory is external read protected

bit 7: **$\overline{CP}$**: Code Protection
1 = Program memory is not code protected
0 = Program memory is code protected

bit 6: **BODEN**: Brown-out Detect Reset Enable bit(1)
1 = BOD Reset enabled
0 = BOD Reset disabled

bit 5: **MCLRE**: $\overline{MCLR}$ Pin Function Select
1 = $\overline{MCLR}$ pin is $\overline{MCLR}$ function
0 = $\overline{MCLR}$ pin is alternate function, $\overline{MCLR}$ function is internally disabled.

bit 4: **$\overline{PWRTE}$**: Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 3: **WDTE**: Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0: **FOSC<2:0>**: Oscillator Selection bits
000 = LP oscillator: Low power crystal on GP5/T1CKI/OSC1/CLKIN and GP4/$\overline{T1G}$/OSC2/CLKOUT
001 = XT oscillator: Crystal/resonator on GP5/T1CKI/OSC1/CLKIN and GP4/$\overline{T1G}$/OSC2/CLKOUT
010 = HS oscillator: High speed crystal/resonator on GP5/T1CKI/OSC1/CLKIN and GP4/$\overline{T1G}$/OSC2/CLKOUT
011 = EC: I/O function on GP4/$\overline{T1G}$/OSC2/CLKOUT, CLKIN on GP5/T1CKI/OSC1/CLKIN
100 = INTOSC oscillator: I/O function on GP4/$\overline{T1G}$/OSC2/CLKOUT, I/O function on GP5/T1CKI/OSC1/CLKIN
101 = INTOSC oscillator: CLKOUT function on GP4/$\overline{T1G}$/OSC2/CLKOUT, I/O function on GP5/T1CKI/OSC1/CLKIN
110 = RC oscillator: I/O function on GP4/$\overline{T1G}$/OSC2/CLKOUT, RC on GP5/T1CKI/OSC1/CLKIN
111 = RC oscillator: CLKOUT function on GP4/$\overline{T1G}$/OSC2/CLKOUT, RC on GP5/T1CKI/OSC1/CLKIN

Note1: Enabling Brown-out Detect Reset Enable does not automatically enable the Power-up Timer Enable (PWRTE).
2: The Bandgap Calibration bits must be read, preserved, then replaced by the user during any bulk erase operation.

Legend			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	1 = bit is set	0 = bit is cleared	x = bit is unknown

3.1 Device ID Word

The device ID word for the PIC12F629/675 is located at 2006h.

TABLE 3-1: DEVICE ID VALUES

Device	Device ID Value	
	Dev	Rev
PIC16F629	00 1111 100	x xxxx
PIC16F675	00 1111 110	x xxxx

4.0 CODE PROTECTION

For PIC12F629/675 devices, once code protection is enabled, all program memory locations, except 0x3FF, read all 0's. The ID locations and the configuration word read out in an unprotected fashion. Further programming is disabled for the entire program memory. Data memory is protected with its own code protect bit ($\overline{CPD}$). It is possible to program the ID locations and the configuration word.

4.1 Disabling Code Protection

It is recommended that the following procedure be performed before any other programming is attempted. It is also possible to turn code protection off (data protect bit = 1) using this procedure. However, all data within the program memory and the data memory will be erased when this procedure is executed, and thus, the security of the data or code is not compromised.

To disable code protect:

a) Read and store OSCCAL and BG bits.
b) Execute LOAD CONFIGURATION (000000).
c) Execute BULK ERASE PROGRAM MEMORY (001001).
d) Wait Tera.
e) Execute BULK ERASE DATA MEMORY (001011).
f) Wait Tera.
g) Reset device to RESET address counter before re-programming device.
h) Restore OSCCAL and BG bits.

Note:	To ensure system security, if $\overline{CPD}$ bit = 0, step c) will also erase data memory.

4.2 Embedding Configuration Word and ID Information in the HEX File

To allow portability of code, the programmer is required to read the configuration word and ID locations from the HEX file when loading the HEX file. If configuration word information was not present in the HEX file, then a simple warning message may be issued. Similarly, while saving a HEX file, configuration word and ID information must be included. An option to not include this information may be provided.

Specifically for the PIC12F629/675, the EEPROM data memory should also be embedded in the HEX file (see Section 4.3.2).

Microchip Technology Incorporated feels strongly that this feature is important for the benefit of the end customer.

4.3 Checksum Computation

4.3.1 CHECKSUM

Checksum is calculated by reading the contents of the PIC12F629/675 memory locations and adding up the opcodes up to the maximum user addressable location, (e.g., 0x3FF for the PIC12F629/675). Any carry bits exceeding 16 bits are neglected. Finally, the configuration word (appropriately masked) is added to the checksum. Checksum computation for each member of the PIC12F629/675 devices is shown in Table 4-1.

The checksum is calculated by summing the following:

- The contents of all program memory locations
- The configuration word, appropriately masked
- Masked ID locations (when applicable)

The Least Significant 16 bits of this sum is the checksum.

The following table describes how to calculate the checksum for each device. Note that the checksum calculation differs depending on the code protect setting. Since the program memory locations read out differently depending on the code protect setting, the table describes how to manipulate the actual program memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire program memory can simply be read and summed. The configuration word and ID locations can always be read.

Note:	Some older devices have an additional value added in the checksum. This is to maintain compatibility with older device programmer checksums.

TABLE 4-1: CHECKSUM COMPUTATION

Device	Code Protect	Checksum*	Blank Value	0x25E6 at 0 and Max Address
PIC12F629/675	OFF	SUM[0x0000:0x3FE] + CFGW & 01FF	BE00	89CE
	ALL	CFGW & 0x01FF + SUM_ID	BF7F	8B4D

Legend: CFGW = Configuration Word
SUM[a:b] = [Sum of locations a to b inclusive]
SUM_ID = ID locations masked by 0xF then made into a 16-bit value with ID0 as the most significant nybble.
For example, ID0 = 0x1, ID1 = 0x2, ID3 = 0x3, ID4 = 0x4, then SUM_ID = 0x1234
*Checksum = [Sum of all the individual expressions] MODULO [0xFFFF]
+ = Addition
& = Bitwise AND

4.3.2 EMBEDDING DATA EEPROM CONTENTS IN HEX FILE

The programmer should be able to read data EEPROM information from a HEX file and conversely (as an option), write data EEPROM contents to a HEX file along with program memory information and fuse information.

The 128 data memory locations are logically mapped starting at address 0x2100. The format for data memory storage is one data byte per address location, LSb aligned.

5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 5-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

		Standard Operating Conditions (unless otherwise stated) Operating Temperature -40°C ≤ TA ≤ +85°C Operating Voltage 4.5V ≤ VDD ≤ 5.5V				
Characteristics	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions/Comments**
General						
VDD level for word operations, program memory	VDD	2.0 4.5		5.5 5.5	V V	PIC12F629/675-ICD PIC12F629/675
VDD level for word operations, data memory	VDD	4.5		5.5	V	
VDD level for bulk erase/write operations, program and data memory	VDD	4.5		5.5	V	
High voltage on $\overline{\text{MCLR}}$ for Programming mode entry	VIHH	VDD + 3.5		13.5	V	
$\overline{\text{MCLR}}$ rise time (VSS to VHH) for Programming mode entry	Tvhhr			1.0	µs	
Hold time after VPP↑	Tppdp	5			µs	
(CLOCK, DATA) input high level	VIH1	0.8 VDD			V	
(CLOCK, DATA) input low level	VIL1	0.2 VDD			V	
CLOCK, DATA setup time before $\overline{\text{MCLR}}$↑ (Programming mode selection pattern setup time)	Tset0	100			ns	
CLOCK, DATA hold time after $\overline{\text{MCLR}}$↑ (Programming mode selection pattern setup time)	Thld0	5			µs	
Serial Program/Verify						
Data in setup time before clock↓	Tset1	100			ns	
Data in hold time after clock↓	Thld1	100			ns	
Data input not driven to next clock input (delay required between command/data or command/command)	Tdly1	1.0			µs	
Delay between clock↓ to clock↑ of next command or data	Tdly2	1.0			µs	
Clock↑ to data out valid (during READ DATA)	Tdly3			80	ns	
Erase cycle time	Tera		4	8	ms	
Programming cycle time	Tprog		4	8	ms	
Time delay from program to compare (HV discharge time)	Tdis	0.5			µs	

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

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Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company’s quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta
500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York
150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

China - Hong Kong SAR
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India
Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan
Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy
Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom
Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

05/01/02

